REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Office Action of August 26, 2004 has been received and its contents carefully reviewed.

Claims 2, 3, 5, 8, 16, 17 are hereby amended and claims 1, 4, and 15 are hereby canceled. Accordingly, claims 2, 3, 5, 6, 8-14, 16, and 17 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

Applicants appreciate the Examiner's indication of allowable subject matter in claim 13.

In the Office Action, the Examiner rejected claims 1-5, 8, and 15-17 under 35 U.S.C. § 102(e) as being anticipated by Tanaka (U.S. Patent No. 5,900,852). This rejection is respectfully traversed and reconsideration is requested.

As set forth in M.P.E.P. § 2131, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single reference. That is, the identical invention must be shown in as complete detail as contained in the claim. Stated another way, the elements shown in the reference must be arranged as required by the claim.

Rejecting claims 2, 5, 15, and 16, however, the Examiner asserts that Tanaka teaches "resetting each liquid crystal cell of the liquid crystal display device simultaneously." Assuming *arguendo* that Tanaka actually discloses what it is alleged to disclose, Applicants respectfully submit Tanaka fails to disclose "wherein resetting each liquid crystal cell of the liquid crystal display device simultaneously comprises applying a reset voltage to a common electrode of the liquid crystal display device," as recited in claim 2, "wherein the reset voltage is applied to a common electrode of the liquid crystal display device," as recited in claim 5, "wherein the means for simultaneously resetting all of the liquid crystal cells comprises means for applying a reset voltage level to the common electrode," as recited in claim 16, and "wherein the means for simultaneously resetting all of the liquid crystal cells comprises means for simultaneously applying a gate high voltage to each gate line," as recited in claim 17. That is, Applicants

respectfully submit that "resetting each liquid crystal cell of the liquid crystal display device simultaneously," as allegedly taught by Tanaka, does not anticipate at least the aforementioned elements recited in claims 2, 5, 16, and 17. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102(e).

Further, in rejecting claims 3 and 8, the Examiner asserts that Tanaka teaches "simultaneously applying a reset voltage to a gate electrode line of each liquid crystal cell." Assuming *arguendo* that Tanaka actually discloses what it is alleged to disclose, Applicants respectfully submit Tanaka fails to disclose "wherein resetting each liquid crystal cell of the liquid crystal display device simultaneously comprises simultaneously applying a gate high voltage to a gate electrode line of each liquid crystal cell," as recited in claim 3, and "wherein the reset voltage is a gate high voltage simultaneously applied to gate electrode lines of the liquid crystal display device," as recited in claim 8. That is, Applicants respectfully submit that "simultaneously applying a reset voltage to a gate electrode line of each liquid crystal cell," as allegedly taught by Tanaka, does not anticipate at least the aforementioned elements recited in claims 3 and 8. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102(e).

In the Office Action, the Examiner rejected claims 6 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of Bird (U.S. Patent No. 5,852,425). This rejection is respectfully traversed and reconsideration is requested.

Claim 6 depends from claim 5. Bird is asserted by the Examiner as disclosing features recited by dependent claim 6. Without reaching the merits of this assertion, Applicants respectfully submit that Bird fails to cure the above-cited deficiency of Tanaka as applied to claim 5 above. Therefore, Applicants submit that the combination of Tanaka in view of Bird fails to render claim 6 obvious under 35 U.S.C. § 103(a). For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

As set forth in M.P.E.P. § 2143.01, the fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient, by itself, to establish *prima facie* obviousness. Similarly, the mere fact that references can be combined does not render the resultant combination obvious unless the reference also suggests the desirability of the

combination. That is, there must be some objective reason to combine the teachings of the references.

Rejecting claim 9, the Examiner acknowledges that Tanaka fails to disclose applying "a common voltage to a common electrode" and relies upon Bird to cure this deficiency. Specifically, the Examiner asserts that Bird teaches "voltage selecting means for selecting, in response to an input control signal, a normal common voltage (Ve high) ... and for selecting, in response to the input control signal, a reset voltage (Ve zero volt) less than the normal common voltage...." Applicants respectfully disagree.

Specifically, at column 8, lines 3-6, Bird states "[d]uring this reset phase, the voltage Ve of the common electrode 15 is held at the same reference level, i.e., zero volts, by the circuit 23" while, at column 8, lines 11-14, Bird merely states "[t]his biasing results from the timing and control circuit 23 switching the common electrode 15 to a higher voltage Vehigh via the line 22 in FIG. 1...." It is respectfully submitted, however, that Bird fails to teach, either expressly or inherently, wherein the timing and control circuit 23 outputs the high and low common voltages Ve cited by the Examiner based on the same control signal as recited in claim 9. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

According to M.P.E.P. § 707.07(f), where Applicants traverse any rejection, the Examiner should, if the rejection is repeated, take note of the Applicants' argument and answer the substance of it. It is respectfully submitted that the argument presented in the preceding paragraphs was previously presented in the Reply under 37 C.F.R. § 1.111 on June 3, 2004. However, the present Office Action does not address the aforementioned deficiency of Bird with respect to claim 9. If the Examiner intends to maintain the present rejection by relying upon Bird, Applicants respectfully request the Examiner take note of all arguments presented and answer the substance them.

In the Office Action, the Examiner rejected claims 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of Yanagi (U.S. Patent No. 6,310,616). This rejection is respectfully traversed and reconsideration is requested.

Rejecting claim 10, the Examiner acknowledges Tanaka fails to disclose "a voltage amplifier for amplifying an input control signal to a common electrode of the liquid crystal display device and, wherein the voltage amplifier outputs a normal common electrode voltage in an interval when a data voltage is charged and maintained in the liquid crystal cells, and outputs a reset voltage less than the normal common electrode voltage in the reset interval."

While Tanaka fails to disclose the subject matter acknowledged above by the Examiner, it is respectfully submitted that such subject matter is not recited in claim 10. To reiterate, claim 10 recites a reset circuit including a voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval, wherein the amplified input control signal is to be applied to a common electrode of the liquid crystal display device. In light of arguments made above with respect to the rejection of claim 9, it is respectfully submitted that Tanaka also fails to teach or suggest the elements actually recited in claim 10.

Attempting to cure the Examiner-acknowledged deficiency of Tanaka, the Examiner cites Yanagi et al. as showing "a voltage amplifier for amplifying an input control signal to a common electrode driver (500; see figure 48) of the liquid crystal display device."

Even if Yanagi et al. shows what it is alleged to show, Applicants respectfully submit Yanagi et al. fails to cure the deficiency of Tanaka with respect to claim 10. Specifically, Yanagi et al. fails to teach or suggest voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval, wherein the amplified input control signal is to be applied to a common electrode of the liquid crystal display device. Given that neither Tanaka nor Yanagi et al. teach or suggest the elements recited in claim 10 (and therefore the elements recited in claim 11), Applicants respectfully submit a *prima facie* case of obviousness has not been established and respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a) for at least this reason.

In concluding with the rejection of claim 10, the Examiner states it would have been obvious to "improve upon the drive circuit [of Tanaka] for a display device, as disclosed by Yanagi" because "[d]oing so would amplify the input control signal and increase the brightness of the display."

According to M.P.E.P. § 2144.02, the rationale to support a rejection under 35 U.S.C. § 103 may rely solely on logic and sound scientific principle. However, when an Examiner relies on a scientific theory, evidentiary support for the existence and meaning of that theory must be provided.

From the Examiner's theory, it appears that improving Tanaka "as disclosed by Yanagi" would enable one of ordinary skill in the art to "increase the brightness of the display," thus rendering the claimed invention obvious.

Applicants respectfully submit, however, evidentiary support for the existence and meaning of the Examiner's theory outlined above must be, but has not been, provided. In the absence of any evidentiary support, Applicants respectfully submit Tanaka and Yanagi et al. have merely been combined using the presently claimed invention as a template via improper hindsight reasoning. For at least this reason, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

As previously mentioned, M.P.E.P. § 707.07(f) states that, where Applicants traverse any rejection, the Examiner should, if the rejection is repeated, take note of the Applicants' argument and answer the substance of it. It is respectfully submitted that the argument presented in the preceding paragraphs was previously presented in the Reply under 37 C.F.R. § 1.111 on June 3, 2004. However, the present Office Action does not address the aforementioned deficiency of Yanagi with respect to claim 10 or the motivational deficiency noted above. If the Examiner intends to maintain the present rejection by relying upon Yanagi, Applicants respectfully request the Examiner take note of all arguments presented and answer the substance them.

In the Office Action, the Examiner rejected claims 12 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. (U.S. Patent No. 6,151,016) in view of Matsushima et al. (U.S. Patent No. 6,396,468). This rejection is respectfully traversed and reconsideration is requested.

In rejecting claim 12, the Examiner cites Kanbe et al. as failing to disclose "level shifters connected individually to outputs of the logical OR gates." Attempting to cure the deficiency of Kanbe et al., the Examiner cites Matsushima et al. as teaching "logic gates (NAND

gates 1024 (fig. 6) of MUX 3b (fig. 4)) having input to level shifter 3c (fig. 4), see also col. 11, lines 67 to col. 12, line 2.

Applicants respectfully submit, however, that Matsushima et al. fails to cure the deficiency of Kanbe et al. Specifically, even if Matsushima et al. teaches logic NAND gates having input to level shifters, such a teaching fails to cure the deficiency of Kanbe et al. with respect to claim 12, i.e., Matsushima et al. fails to teach or even suggest level shifters connected to outputs of logical OR gates. For at least this reason, Applicants request withdrawal of the present rejection of claims 12 and 14, which depends from claim 12, under 35 U.S.C. § 103(a).

In concluding the rejection of claim 12, the Examiner concludes it would have been obvious to "improve upon the erasing device" of Kanbe et al. because "[d]oing so would provide an erasing device for a LCD image which can erase an afterimage quickly while suppressing the deterioration of the liquid crystal, and to provide a LCD device including such an erasing device."

It is respectfully submitted that, even if it would have been obvious to improve upon the erasing device disclosed by Kanbe et al. to "provide an erasing device for a LCD image which can erase an afterimage quickly while suppressing the deterioration of the liquid crystal, and to provide a LCD device including such an erasing device," the Examiner has failed to establish that such improvement may be obtained in light of the claimed combination of elements (i.e., a shift register, logical OR gates performing a logical OR operation of an input reset signal and each gate driving signal from the shift register, and level shifters connected individually to outputs of the logical OR gates). In addition, similar arguments presented above with respect to the Examiner's theory of improving Tanaka in the rejection of claim 10 are equally applicable in the present rejection. For at least these reasons, Applicants respectfully request withdrawal of the present rejection of claims 12 and 14, which depends from claim 12, under 35 U.S.C. § 103(a).

As previously mentioned, M.P.E.P. § 707.07(f) states that, where Applicants traverse any rejection, the Examiner should, if the rejection is repeated, take note of the Applicants' argument and answer the substance of it. It is respectfully submitted that the argument presented in the preceding paragraphs was previously presented in the Reply under 37 C.F.R. § 1.111 on

June 3, 2004. However, the present Office Action does not address any of Applicants arguments associated with this rejection. If the Examiner intends to maintain the present rejection, Applicants respectfully request the Examiner take note of all arguments presented and answer the substance them.

In view of the amendments and arguments presented above, Applicants believe each of the presently pending claims in this application to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these paper are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: November 30, 2004

Respectfully submitted,

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Dated: November 30, 2004

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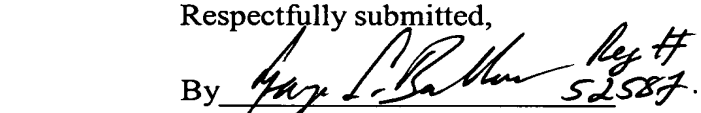
By  Reg # 52587.

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